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APPENDIX ON APPEAL

1-15 (canceled)

16. A method of operating a parallel computer system having at least first and second processor elements, each processor element comprising a processor, a local program memory, a local data memory, a communications manager and an operating system, within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network; the processor elements each executing an application; each communications manager further containing a plurality of predefined values each of which, in the event of a match of one of the predetermined values to a global address in a message, causes storage of results of an associated computation in local data memory; the method comprising the steps of:

writing, by the processor of the first processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element;

adding, by the communications manager, a global address to the result of the computation;

propagating, on the message-passing communications network, a message comprising the

global address and the result of the computation;

receiving the message, via the message-passing communications network, by the communications manager of the second processor element;

comparing, by the communications manager of the second processor element, the global address in the message with the predefined values for a match;

in the event of a match, computing a local address by the communications manager of the second processor element, and storing the results of the computation at the local address via the common bus to the local data memory.

17. The method of claim 16 wherein the predefined values are further characterized as comprising an address window, each window comprising an initial address and an end address, a match comprising the global address falling between the initial address and the end address.

18. The method of claim 16 wherein computing a local address comprises adding an offset of one or more bits to the global address, yielding the local address.

19. The method of claim 16 wherein computing a local address comprises replacing one or more bits of the global address by a base value, yielding the local address.

20. The method of claim 16 wherein the propagating step comprises propagating the message to a number of processor elements, the number comprising less than all and more than one of the processor elements.

21. A parallel computer system having at least first and second processor elements, each processor element comprising a processor, a local program memory, a local data memory, a communications manager and an operating system, within each processor

element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; the local data memories of the at least first and second processor elements not on a common bus; the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network; the processor elements each executing an application; each communications manager further containing a plurality of predefined values each of which, in the event of a match of one of the predetermined values to a global address in a message, causes storage of results of an associated computation in local data memory;

for each communications manager, the communications manager comprising first means responsive to writing, by the processor of the processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element, by adding a global address to the result of the computation, and by propagating, on the message-passing communications network, a message comprising the global address and the result of the computation;

for each communications manager, the communications manager comprising second means responsive to receiving a message, via the message-passing communications network, by the communications manager, for comparing the global address in the message with the plurality of predefined values for a match, in the event of a match, for computing a local address, and storing the results of the computation at the local address via the common bus to the local data memory.

22. The apparatus of claim 21 wherein the predefined values are further characterized as comprising an address window, each window comprising an initial address and an end address, a match comprising the global address falling between the initial address and the end address.

23. The apparatus of claim 21 wherein the second means computes a local address by

adding an offset of one or more bits to the global address, yielding the local address.

24. The apparatus of claim 21 wherein the second means computes a local address by replacing one or more bits of the global address by a base value, yielding the local address.

25. The apparatus of claim 21 wherein the first means propagates the message to a number of processor elements, the number comprising less than all and more than one of the processor elements.

26. A method of operating a parallel computer system having at least first and second processor elements, each processor element comprising a processor, a local program memory, a local data memory, a communications manager and an operating system, within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network; the processor elements each executing an application; each communications manager further containing a plurality of predefined values each of which, in the event of a match of one of the predetermined values to a global address in a message, causes storage of results of an associated computation in local data memory; the method comprising the steps of:

writing, by the processor of the first processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element;

adding, by the communications manager, a global address to the result of the computation;

propagating, on the message-passing communications network, a message comprising the

global address and the result of the computation;

receiving the message, via the message-passing communications network, by the communications manager of the second processor element;

comparing, by the communications manager of the second processor element, the global address in the message with the predefined values for a match;

in the event of a match, computing a local address by the communications manager of the second processor element, and storing the results of the computation at the local address via the common bus to the local data memory,

wherein the predefined values are further characterized as comprising an address window, each window comprising an initial address and an end address, a match comprising the global address falling between the initial address and the end address.

27. A method of operating a parallel computer system having at least first and second processor elements, each processor element comprising a processor, a local program memory, a local data memory, a communications manager and an operating system, within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network; the processor elements each executing an application; each communications manager further containing a plurality of predefined values each of which, in the event of a match of one of the predetermined values to a global address in a message, causes storage of results of an associated computation in local data memory; the method comprising the steps of:

writing, by the processor of the first processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of

the first processor element;

adding, by the communications manager, a global address to the result of the computation;

propagating, on the message-passing communications network, a message comprising the global address and the result of the computation;

receiving the message, via the message-passing communications network, by the communications manager of the second processor element;

comparing, by the communications manager of the second processor element, the global address in the message with the predefined values for a match;

in the event of a match, computing a local address by the communications manager of the second processor element, and storing the results of the computation at the local address via the common bus to the local data memory,

wherein the propagating step comprises propagating the message to a number of processor elements, the number comprising less than all and more than one of the processor elements.

28. A parallel computer system having at least first and second processor elements, each processor element comprising a processor, a local program memory, a local data memory, a communications manager and an operating system, within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; the local data memories of the at least first and second processor elements not on a common bus; the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network; the processor elements each

executing an application; each communications manager further containing a plurality of predefined values each of which, in the event of a match of one of the predetermined values to a global address in a message, causes storage of results of an associated computation in local data memory;

for each communications manager, the communications manager comprising first means responsive to writing, by the processor of the processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element, by adding a global address to the result of the computation, and by propagating, on the message-passing communications network, a message comprising the global address and the result of the computation;

for each communications manager, the communications manager comprising second means responsive to receiving a message, via the message-passing communications network, by the communications manager, for comparing the global address in the message with the predefined values for a match, in the event of a match, for computing a local address, and storing the results of the computation at the local address via the common bus to the local data memory,

wherein the predefined values are further characterized as comprising an address window, each window comprising an initial address and an end address, a match comprising the global address falling between the initial address and the end address.

29. A parallel computer system having at least first and second processor elements, each processor element comprising a processor, a local program memory, a local data memory, a communications manager and an operating system, within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; the local data memories of the at least first and second processor elements not on a common bus; the communications managers of the at least first and second processor elements communicatively coupled by

means of a message-passing communications network; the processor elements each executing an application; each communications manager further containing a plurality of predefined values each of which, in the event of a match of one of the predetermined values to a global address in a message, causes storage of results of an associated computation in local data memory;

for each communications manager, the communications manager comprising first means responsive to writing, by the processor of the processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element, by adding a global address to the result of the computation, and by propagating, on the message-passing communications network, a message comprising the global address and the result of the computation;

for each communications manager, the communications manager comprising second means responsive to receiving a message, via the message-passing communications network, by the communications manager, for comparing the global address in the message with the predefined values for a match, in the event of a match, for computing a local address, and storing the results of the computation at the local address via the common bus to the local data memory,

wherein the first means propagates the message to a number of processor elements, the number comprising less than all and more than one of the processor elements.

30. The method of claim 16 wherein the predefined values are further characterized as comprising at least two address windows, each window comprising an initial address and an end address, a match comprising the global address falling between the initial address and the end address of at least one of the at least two address windows.

31. The apparatus of claim 21 wherein the predefined values are further characterized as comprising at least two address windows, each window comprising an initial address and

an end address, a match comprising the global address falling between the initial address and the end address of at least one of the at least two address windows..

32. (canceled)

33. A method of operating a parallel computer system having at least first and second processor elements, each processor element comprising a processor, a local program memory, a local data memory, a communications manager and an operating system, within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network and not solely by a common bus; the processor elements each executing an application; each communications manager further containing a plurality of predefined values each of which, in the event of a match of one of the predetermined values to a global address in a message, causes storage of results of an associated computation in local data memory; the method comprising the steps of:

writing, by the processor of the first processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element;

adding, by the communications manager, a global address to the result of the computation;

propagating, on the message-passing communications network and not solely by a common bus, a message comprising the global address and the result of the computation;

receiving the message, via the message-passing communications network and not solely by a common bus, by the communications manager of the second processor element;

comparing, by the communications manager of the second processor element, the global address in the message with the predefined values for a match;

in the event of a match, computing a local address by the communications manager of the second processor element, and storing the results of the computation at the local address via the common bus to the local data memory.

34. A parallel computer system having at least first and second processor elements, each processor element comprising a processor, a local program memory, a local data memory, a communications manager and an operating system, within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; the local data memories of the at least first and second processor elements not on a common bus; the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network; the processor elements each executing an application; each communications manager further containing a plurality of predefined values each of which, in the event of a match of one of the predetermined values to a global address in a message, causes storage of results of an associated computation in local data memory;

for each communications manager, the communications manager comprising first means responsive to writing, by the processor of the processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element, by adding a global address to the result of the computation, and by propagating, on the message-passing communications network and not solely by a common bus, a message comprising the global address and the result of the computation;

for each communications manager, the communications manager comprising second

means responsive to receiving a message, via the message-passing communications network and not solely by a common bus, by the communications manager, for comparing the global address in the message with the plurality of predefined values for a match, in the event of a match, for computing a local address, and storing the results of the computation at the local address via the common bus to the local data memory.